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APPLICATION FOR LETTERS PATENT

Collective Automatic Gain Control

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CROSS-REFERENCES TO RELATED APPLICATIONS

This U.S. Nonprovisional Patent Application is a continuation of Application No. 10/444,175, filed on May 23, 2003, which is a divisional application of Application No. 09/891,577, filed on June 25, 2001 (now U.S. Patent 6,600,374).

TECHNICAL FIELD

The invention relates to automatic gain control in signal receivers.

BACKGROUND

High-speed digital systems such as memory systems sometimes use a form of I/O in which data is defined by a differential voltage signal. A differential voltage signal comprises a pair of complementary signals. A high logic level is represented by setting a first of the signals to a relatively high voltage and the second of the signals to a relatively low voltage. A low logic level is represented by switching the two voltages, so that the first signal has a relatively lower voltage than the second signal. Differential signaling is advantageous because of its relative immunity to noise and other signal degradations. A disadvantage of differential signaling is that it requires two signal lines for every data bit.

In order to reduce the number of data signaling lines, single-ended signaling is often used in high speed circuits. This particular type of signaling is non-differential, although it is sometimes referred to as "pseudo differential" signaling. Pseudo differential signaling specifies logic levels as voltages relative to a common, intermediate reference voltage. For example, a signal might be defined to represent a high logic level whenever its voltage is above the reference

1 voltage, and to represent a low logic level whenever its voltage is below the
2 reference voltage. This type of signaling requires fewer conductors than
3 differential signaling, because a single reference line can be used in conjunction
4 with many data signal lines. Although this type of signaling is less immune to
5 signal degradation than differential signaling, it represents a distinct improvement
6 over signaling systems in which signal levels are specified in terms of absolute
7 voltages, rather than in relation to a specified reference voltage. Typically, a
8 reference voltage signal is transmitted alongside data signals so that the same
9 sources of noise will affect both the reference signal and the data signals. This
10 tends to cancel the effects of the noise and provides some degree of noise
11 immunity.

12 Regardless of whether signals are differential or non-differential, it is
13 frequently desirable to perform some sort of signal buffering and/or conditioning
14 at the receiving device. This is typically accomplished by a data receiver
15 corresponding to each incoming signal line.

16 Fig. 1 shows a data receiver 10 that buffers an incoming data signal D_{IN} to
17 form a buffered or amplified internal data signal D_{OUT} . This circuit uses automatic
18 gain control to achieve a desired voltage amplitude at D_{OUT} .

19 Data receiver 10 comprises a variable gain amplifier 12 that receives D_{IN}
20 and produces D_{OUT} . The receiver also has an envelope detector 14 that detects the
21 voltage amplitude of signal D_{OUT} . An envelope detector or peak detector is a well-
22 known type of circuit whose output voltage tracks the peak or swing voltages of a
23 modulating input voltage such as a data signal.

24 Fig. 2 shows a simplified example of an envelope detector 14, comprising
25 an FET control transistor M, a tracking capacitance C, a charging current source

1 I_{CH} , and a discharging current source I_{DIS} . Transistor M is controlled by data
2 signal D_{OUT} to charge capacitance C whenever D_{OUT} is relatively high. When the
3 voltage V_{ENV} on capacitance C approaches the voltage of D_{OUT} , the transistor shuts
4 off because of the reduced gate-to-source voltage of the transistor in this condition.
5 Thus, the transistor charges capacitance C to approximately the “high” logic level
6 of D_{OUT} . The size of current source I_{CH} determines the “attack” rate of the
7 envelope detector—the rate at which output voltage V_{ENV} will climb in response to
8 an increased voltage at D_{OUT} . Current source I_{DIS} is connected to slowly discharge
9 capacitance C, to account for situations in which the peak levels of D_{IN} decrease
10 over time. The size of current source I_{DIS} determines the “decay” rate of the
11 envelope detector—the rate at which output voltage V_{ENV} will fall in response to a
12 decreased input voltage D_{OUT} . I_{DIS} is chosen to be small enough so that the voltage
13 at D_{OUT} will remain close to its peak value between peaks that occur in D_{IN} .

14 If appropriate sizes are selected for current sources I_{CH} and I_{DIS} , an
15 envelope detector can be configured to produce an output that closely tracks the
16 peak voltages of a data signal. Although the envelope detector of Fig. 2 is
17 configured to detect positive signal peaks, the circuit can be easily altered to detect
18 negative peaks in an input signal.

19 Referring again to Fig. 1, envelope detector 14 is configured to determine
20 and track the peak voltage of output signal D_{OUT} , and to produce a voltage signal
21 V_{ENV} representing this peak voltage. A feedback component 20 receives V_{ENV} and
22 compares it to a supplied reference amplitude V_{AMP} . The output of feedback
23 component 20 is connected to the gain control of amplifier 12, forming a feedback
24 loop that operates to minimize any difference between the peak output V_{ENV} of
25 signal D_{OUT} and the supplied amplitude reference V_{AMP} . In other words, this

1 circuit sets the gain of amplifier 12 so that the peak voltage of output D_{OUT} is
2 approximately equal to the voltage of V_{AMP} . In implementation, feedback
3 component 20 is a g_m stage whose output increases or decreases depending on the
4 relative values of its inputs.

5 Fig. 3 shows data receiver 10, with the generic representation of amplifier
6 12 of Fig. 1 being replaced by a more detailed implementation of a differential
7 amplifier circuit. Such a differential amplifier is typically used in conjunction
8 with an input an input data signal D_{IN} that is specified relative to an intermediate
9 reference voltage V_{REF} , which is relatively constant. The differential amplifier
10 produces a differential voltage output D_{OUT} having + and – outputs.

11 The differential amplifier comprises a differential pair of FET transistors
12 M_2 and M_3 , whose sources are connected in common. The drains of M_2 and M_3
13 form the high and low outputs of differential voltage output signal D_{OUT} , and are
14 connected through respective loads $R1_{LOAD}$ and $R2_{LOAD}$ to a high supply voltage
15 V_{dd} . The gates of M_2 and M_3 are connected respectively to D_{IN} and V_{REF} . The
16 sources of M_2 and M_3 are connected in common through a biasing current source
17 I_{BIAS} to a low supply voltage V_{ss} .

18 The input of envelope detector 14 is connected to the positive side of
19 differential output D_{OUT} . The output of feedback component 20 controls current
20 source I_{BIAS} , which in turn controls the gain of the amplifier circuit. Feedback
21 component 20 receives the output of envelope detector 14 and the amplitude
22 reference V_{AMP} , and therefore establishes the gain of the amplifier circuit so that
23 the peak voltage of output signal D_{OUT} is approximately equal to V_{AMP} .

24 The circuits described above have been used with success in many
25 situations. However, problems arise in certain situations. One problem arises

1 from the use of automatic gain control and envelope detectors in situations where
2 there are relatively long periods without a transition in the received data signal.
3 For example, a relatively long period in which a data signal remains low results in
4 a decaying envelope voltage, which in turn causes automatic gain control circuits
5 to inappropriately increase circuit gains. Furthermore, in many cases it is
6 challenging to determine the optimal amplitude of D_{OUT} . It is desirable to keep the
7 amplitude as low as possible to reduce power consumption, but also to keep it as
8 high as necessary to ensure accurate differentiation between high and low signals.

9 A further concern arises where a data signal is precisely timed relative to
10 other signals. In cases such as this, it is important to maintain the relative timing
11 between the two or more signals. However, variations in amplification can affect
12 this timing. This problem arises, for example, with incoming signals that must
13 exceed a certain threshold voltage in order for them to be resolved by receiving
14 circuitry. In a situation like this, a signal having a relatively higher amplitude will
15 be resolved more quickly than a signal having a relatively lower amplitude. Thus,
16 differences in amplification between two signals will be perceived as timing
17 differences by receiving circuitry.

18 Differences in duty cycles between two signals can also affect their relative
19 timings as perceived by receiving circuitry. This problem can arise in situations
20 where one signal is a true differential voltage signal and the other is a non-
21 differential or pseudo-differential voltage signal. A differential voltage signal
22 typically achieves very close to a 50% duty cycle, even after amplification. Non-
23 differential signals, however, are often subject to disproportionate amplification
24 with respect to the positive and sides of their waveforms. This is especially true in
25 circuits where reduced supply voltages are employed in order to increase circuit

1 speeds. In such circuits, current sources sometimes begin to operate below
2 saturation, typically reducing the amount of amplification applied to negative
3 portions of waveforms. This has the effect of changing the duty cycle of an
4 amplified signal, which also changes the relative point in time at which the signal
5 crosses specified voltage thresholds.

6 The circuits and techniques described below address these and other issues.

7 8 **BRIEF DESCRIPTION OF THE DRAWINGS**

9 Fig. 1 is a schematic diagram of a prior art automatic gain control circuit.

10 Fig. 2 is a schematic diagram of an envelope detection circuit.

11 Fig. 3 is a schematic diagram of a prior art automatic gain control circuit.

12 Figs. 4 and 5 are schematic diagrams of an automatic gain control circuit in
13 which the envelope of an amplified data signal is adjusted to equal the envelope of
14 a related clock signal.

15 Fig. 6 is a schematic diagram of a receiver circuit employing group
16 envelope detection techniques.

17 Figs. 7 and 8 are schematic diagrams showing examples of group envelope
18 detection circuitry.

19 Fig. 9 is a schematic diagram of a receiver circuit employing group
20 envelope detection techniques.

21 Fig. 10 is a schematic diagram illustrating group envelope detection applied
22 to groups or bytes of data signals.

23 Fig. 11 is a schematic diagram illustrating techniques for correcting
24 asymmetries in differential voltage output signals.
25

1 Fig. 12 is a graph illustrating asymmetries that can occur in prior art
2 differential amplifier circuits.

3 Fig. 13 is a schematic diagram illustrating the use of a plurality of
4 differential amplifiers such as the one shown in Fig. 11.

5 Fig. 14 is a schematic diagram illustrating circuits for operating the
6 previously discussed circuits in situations where gains are calibrated in calibration
7 procedures and stored for later use when receiving signals from different senders.

8 Fig. 15 is a schematic diagram of a g_m stage suitable for use in the
9 embodiments described above.

10 11 **DETAILED DESCRIPTION**

12 The following description sets forth specific embodiments of circuits and
13 techniques that incorporate elements recited in the appended claims. The
14 embodiments are described with specificity in order to meet statutory
15 requirements. However, the description itself is not intended to limit the scope of
16 this patent. Rather, the inventors have contemplated that the claimed invention
17 might also be embodied in other ways, to include different elements or
18 combinations of storage elements similar to the ones described in this document,
19 in conjunction with other present or future technologies.

20 Fig. 4 shows one embodiment of a receiver circuit 40. The signal receiver
21 receives a data signal D_{IN} and produces an amplified data output signal D_{OUT} . The
22 input data signal D_{IN} is timed relative to a clock signal CLOCK.

23 Receiver circuit 40 comprises an amplifier 42 having a variable gain. The
24 amplifier receives data input signal D_{IN} and produces amplified data output signal
25 D_{OUT} .

1 Receiver circuit 40 implements automatic gain control with respect to its
2 received data signal. The automatic gain control is implemented in part by signal
3 envelope detection circuitry 44 that is responsive to the amplified data output
4 signal D_{OUT} to indicate an amplified signal envelope voltage VO_{ENV} . VO_{ENV}
5 tracks the voltage swing or peak voltage of D_{OUT} . Fig. 2 shows a simplified
6 example of an appropriate envelope detector.

7 The automatic gain control of circuit 40 also comprises clock envelope
8 detection circuitry 45 responsive to clock signal $CLOCK$ to indicate a clock
9 envelope voltage VC_{ENV} . VC_{ENV} tracks the voltage swing or peak voltage of clock
10 signal $CLOCK$. Again, Fig. 2 shows a simplified example of an appropriate
11 envelope detector.

12 Automatic gain control circuitry further includes a feedback component 46
13 configured to adjust the gain of amplifier 42 as a function of the difference
14 between the amplified signal envelope voltage VO_{ENV} and the clock envelope
15 voltage VC_{ENV} . More specifically, the feedback component has negative and
16 positive inputs that receive VO_{ENV} and VC_{ENV} , respectively, and in response
17 produces a signal V_D that changes depending on the relative values of VO_{ENV} and
18 VC_{ENV} . A component such as this is typically referred to as a g_m stage. By
19 connecting V_D to the gain control input of amplifier 42, the amplifier gain is
20 controlled in a way that reduces or minimizes any difference between VO_{ENV} and
21 VC_{ENV} , effectively setting the envelope, swing, or amplitude of D_{OUT} to that of
22 clock signal $CLOCK$.

23 This circuit is especially beneficial in systems where received data signals
24 are single-ended, non-differential signals and that are timed relative to a
25 differential voltage clock signal. Typically, the differential nature of the clock

1 signal allows it to be conditioned more effectively than single-ended inputs and for
2 its swing or amplitude to be set with precision to an optimum value. With the
3 circuit of Fig. 4, the effort in conditioning the clock signal can be leveraged to
4 determine and establish an optimum amplitude for buffered received data signals.
5 Furthermore, setting the amplitude of received data signals to match that of the
6 clock signal reduces timing or skew mismatches between the two types of signals,
7 which might otherwise arise because of differing amounts of amplification being
8 introduced in the different signals.

9 A further advantage of this circuit is that a reduced power mode can be
10 implemented simply by reducing the amplitude of $V_{C_{ENV}}$. Reducing the amplitude
11 of $V_{C_{ENV}}$ decreases the gain applied by amplifier 42, thereby reducing power
12 consumption.

13 Fig. 5 shows an embodiment of data receiver 40 in which the generic
14 representation of amplifier 42 in Fig. 4 has been replaced by a more detailed
15 implementation of a differential amplifier circuit. Such a differential amplifier is
16 appropriate for use in conjunction with an input data signal D_{IN} that is specified
17 relative to a relatively constant, intermediate reference voltage V_{REF} . The
18 differential amplifier produces a differential voltage output D_{OUT} having + and -
19 outputs.

20 The differential amplifier comprises a differential pair of FET transistors
21 M_4 and M_5 whose sources are connected in common. The drains of M_4 and M_5
22 form the high and low outputs of differential voltage output signal D_{OUT} , and are
23 connected through respective loads $R_{3_{LOAD}}$ and $R_{4_{LOAD}}$ to a high supply voltage
24 V_{dd} . The gates of M_4 and M_5 are connected respectively to D_{IN} and V_{REF} . The
25

1 sources of M_4 and M_5 are connected in common through a biasing current source
2 I_{BIAS} to a low supply voltage V_{SS} .

3 The input of envelope detector 44 is connected to the positive side of
4 differential output D_{OUT} . The input of envelope detector 45 is connected to one
5 end of differential voltage clock signal $CLOCK$. The outputs of the detectors 44
6 and 45 are connected to the positive and negative inputs, respectively, of a
7 feedback component 46, such as a g_m stage as discussed above. The output of
8 feedback component 46 controls current source I_{BIAS} , which in turn controls the
9 gain of the amplifier circuit. This configuration establishes the gain of the
10 amplifier circuit so that the peak voltage or swing of output signal D_{OUT} is
11 approximately equal to the peak voltage or swing of clock signal $CLOCK$.

12 Fig. 6 shows another embodiment of a signal receiver, generally designated
13 by reference numeral 50. In this example, signal receiver 50 receives a plurality of
14 voltage data signals D_{IN} . For each data signal D_{IN} , signal receiver 50 has a
15 corresponding amplifier 52. The amplifiers receive respective data signals D_{IN} and
16 produce corresponding amplified data signals D_{OUT} . The amplifiers have variable
17 gains.

18 Receiver 50 has group envelope detection circuitry that is responsive to the
19 collective amplified data signals D_{OUT} to indicate a group envelope voltage. In
20 this example, the group envelope detection circuitry comprises a plurality of
21 individual envelope detectors 54 whose capacitive outputs are connected in
22 common to form a group envelope voltage signal VG_{ENV} . In this configuration,
23 the detection circuitry is responsive to peaks in any of data output signals D_{OUT} ,
24 and VG_{ENV} generally tracks the most extreme peaks occurring at any moment on
25 any of the data output signals.

1 The group envelope detection circuitry can be implemented in different
2 ways. One implementation is shown in Fig. 7, where two envelope detectors 54a
3 and 54b have outputs connected in common. Although Fig. 7 shows only two
4 individual detectors, any number of detectors can be configured together in this
5 manner. As discussed with reference to Fig. 2, each detector includes a FET
6 control transistor M, a tracking capacitance C, a charging current source I_{CH} , and a
7 discharging current source I_{DIS} . Each circuit works as already described with
8 reference to Fig. 2. The capacitive outputs of all such individual circuits are
9 connected in parallel to form $V_{G_{ENV}}$.

10 Fig. 8 shows another configuration, in which the tracking capacitance C
11 and discharging current source I_{DIS} are shared. There is a charging current source
12 I_{CH} and control transistor M associated with each data signal D_{OUT} . However,
13 these components are connected in common to charge a single capacitance C.
14 Again, any number of detectors can be connected together in such a fashion.

15 In either of these embodiments, it is possible to choose current source and
16 capacitance sizes so that the overall circuit works in a roughly OR'ed fashion,
17 reflecting the most extreme peak occurring at any moment on any of the data
18 output signals, subject to attack and decay times that depend on the actual circuit
19 implementation. The circuit output can alternatively be viewed as presenting the
20 average of the peak voltages of the data signals D_{OUT} . Although these circuits as
21 shown are appropriate for tracking positive envelopes or peaks, inverse
22 implementations can easily be designed for detecting negative envelopes or peaks.

23 Referring now again to Fig. 6, group envelope voltage $V_{G_{ENV}}$ is provided
24 to the negative input of a feedback component 60, such as a g_m stage as discussed
25 above. An amplitude reference signal is supplied to the positive input of feedback

1 component 60. The output of feedback component 60 is connected in parallel to
2 all of amplifiers 52 to control their gains. Feedback component 60 thus forms
3 feedback that adjusts the amplifier gains as a function of the difference between
4 group envelope voltage $V_{G_{ENV}}$ and supplied amplitude reference V_{AMP} . More
5 specifically, the feedback adjusts the amplifier gains to reduce or minimize the
6 difference between group envelope voltage $V_{G_{ENV}}$ and supplied amplitude
7 reference V_{AMP} .

8 In accordance with the technique described with reference to Fig. 4, V_{AMP}
9 can be derived from a clock signal $CLOCK$ that is used for timing transfer of
10 information on data signals D_{IN} . A reference or clock envelope detector 62
11 receives the clock signal, which can be either a differential voltage signal or a non-
12 differential voltage signal, and produces V_{AMP} as a reference or clock envelope
13 voltage. As already described, V_{AMP} is used as feedback in combination with
14 $V_{G_{ENV}}$, so that the group envelope voltage is set to the approximate envelope
15 voltage of clock signal $CLOCK$.

16 The multi-amplifier circuit of Fig. 6 is preferably duplicated for the data
17 lines of each data group, data byte or data word, with the exception of clock
18 envelope detector 62 whose output is used in common by all such circuits. Thus,
19 within a single data byte or word, each signal line is subject to the same
20 amplification. Furthermore, the gains applied to the respective data groups are
21 adjusted so that their group envelopes match a common reference—in this case the
22 envelope of the clock signal against which the data signals are timed.

23 This technique is a significant improvement over the prior art. Specifically,
24 this circuit exhibits improved response in situations where a single data input
25 might remain unchanged for a relatively long period. In prior art circuits, an

1 individual envelope detector would have begun to decay during this period, and
2 automatic gain control would have responded by inappropriately increasing the
3 circuit gain. In the circuit of Fig. 6, however, this likelihood is reduced by a factor
4 of N , where N is the number of data inputs that are collectively monitored by
5 group envelope detector circuitry 54. Activity on any one of these inputs prevents
6 the decay of the envelope voltage, and thus prevents the automatic gain control
7 feedback from inappropriately increasing the circuit gain.

8 Furthermore, the techniques employed by the circuit of Fig. 6 minimize
9 signal skew within data signals. In particular, the circuit of Fig. 6 results in the
10 same gain being applied to all of the individual data lines of a data byte or data
11 word. This minimizes line-to-line variations in signal skew, and accordingly
12 increases the reliability of the signals. Byte-to-byte skew is also reduced by the
13 technique of adjusting the gains of each byte to a common reference.

14 Fig. 9 shows the signal receiver 50 with specific implementations shown
15 for individual amplifiers 52. These differential amplifiers are appropriate for use
16 in conjunction with input data signals D_{IN} that are specified relative to a relatively
17 constant, intermediate, common reference voltage V_{REF} . In response to D_{IN} and
18 V_{REF} , each differential amplifier produces a differential voltage output signal D_{OUT}
19 having + and - outputs.

20 Each differential amplifier 52 comprises a differential pair of FET
21 transistors M_6 and M_7 whose sources are connected in common. The drains of M_6
22 and M_7 form the high and low outputs of differential voltage output signal D_{OUT} ,
23 and are connected through respective loads $R5_{LOAD}$ and $R6_{LOAD}$ to a high supply
24 voltage V_{dd} . The gates of M_6 and M_7 are connected respectively to D_{IN} and V_{REF} .
25

1 The sources of M_6 and M_7 are connected in common through a biasing current
2 source I_{BIAS} to a low supply voltage V_{ss} .

3 The group envelope detection circuitry is depicted in Fig. 9 as a single
4 group envelope detector 54 that receives the positive side of differential D_{OUT} from
5 each amplifier 52. The output of group envelope detector 54 is connected to the
6 positive input of feedback component 60. The circuit also includes clock envelope
7 detector 62 whose output is connected to the negative input of feedback
8 component 60. The output of feedback component 60 is connected in parallel to
9 control the current sources I_{BIAS} of the different amplifiers 52. Thus, the
10 amplifiers are controlled to all have the same gain—a gain that produces a group
11 envelope approximately equal to that of the clock signal $CLOCK$.

12 Fig. 10 shows yet another embodiment of a signal receiver, generally
13 referenced by numeral 70. This embodiment is similar to that shown in Fig. 6,
14 except that the data input signals D_{IN} are segregated into groups such as data bytes
15 or words. Fig. 10 shows two such groups: Byte A and Byte B.

16 Signal receiver 70 includes groups of amplifiers corresponding respectively
17 to the groups of input signals D_{IN} . The amplifiers produce corresponding groups
18 of amplified data signals D_{OUT} . The amplifiers have variable gains.

19 A group envelope detector 76 is associated with each group of amplified
20 data signals D_{OUT} . Each group envelope detector is responsive to its associated
21 group of amplified data signals D_{OUT} to indicate a group envelope voltage VG_{ENV}
22 for that group of signals D_{OUT} . Group envelope detectors are implemented in
23 accordance with the techniques already described.

24 Receiver 70 comprises feedback associated with each group of amplifiers.
25 The feedback comprises a g_m stage 78 that collectively adjusts the gains of the

1 associated amplifiers as a function of the difference between the group envelope
2 voltage $V_{G_{ENV}}$ of the amplifiers and a supplied amplitude reference V_{AMP} .

3 In this embodiment, V_{AMP} comprises the envelope or peak voltage of a
4 clock signal with which data signals D_{IN} are timed. Specifically, the receiver
5 comprises a clock envelope detector 79 that receives clock signal $CLOCK$ and that
6 in response produces clock envelope voltage signal V_{AMP} . Each of feedback
7 components 78 receives the same clock envelope voltage signal V_{AMP} .

8 Fig. 11 illustrates a further technique that can be used to condition received
9 data signals. The circuit shown in Fig. 11 addresses a problem that sometimes
10 arises in amplifier circuits such as those shown in Figs. 3, 5, and 9. These
11 amplifiers accept differential inputs and produce differential outputs. However,
12 the inputs D_{IN} and V_{REF} are not truly differential, in that V_{REF} is actually a constant
13 voltage while D_{IN} varies above and below V_{REF} . This can cause asymmetries in
14 the amplified output signals. These asymmetries become acute when supply
15 voltages are reduced to achieve higher operating speeds, creating situations in
16 which certain transistors fail to reach saturation.

17 Fig. 12 illustrates this anomaly, showing the voltage outputs of D^{+}_{OUT} and
18 D^{-}_{OUT} in response to an oscillating input D_{IN} . It is apparent that the negative peak
19 V_1 of D^{+}_{OUT} is significantly lower than the negative peak V_2 of D^{-}_{OUT} . The circuit
20 of Fig. 11 corrects this.

21 In the circuit of Fig. 11, a receiver 80 comprises a differential amplifier
22 having two stages of amplification. A first amplification stage is similar to the
23 double-ended differential amplifiers already discussed, being responsive to a data
24 signal D_{IN} and an intermediate reference voltage V_{REF} to produce positive and
25 negative differential output signals D^{+}_{OUT} and D^{-}_{OUT} .

1 More specifically, the first amplification stage comprises a differential pair
2 of transistors M_{10} and M_{11} , corresponding loads R_{7_LOAD} and R_{8_LOAD} , and a biasing
3 current source referred to in Fig. 11 as I_{A_BIAS} . The sources of transistors M_{10} and
4 M_{11} are connected in common and through I_{A_BIAS} to lower supply voltage V_{ss} .
5 The drains of transistors M_{10} and M_{11} are connected respectively through loads
6 R_{7_LOAD} and R_{8_LOAD} to upper supply voltage V_{dd} . The gate of transistor M_{10} is
7 connected to data input signal D_{IN} , while the gate of transistor M_{11} is connected to
8 intermediate voltage reference V_{REF} . Transistors M_{10} and M_{11} produce an
9 amplified differential voltage output signal D_{OUT} comprising first and second
10 output signals referred to as D^{+}_{OUT} and D^{-}_{OUT} . The + component of D_{OUT} is
11 generated at the drain of transistor M_{10} . The – component of D_{OUT} is generated at
12 the drain of transistor M_{11} . The gain of the first amplification stage is adjustable
13 by adjusting the magnitude of current produced by current source I_{A_BIAS} .

14 Receiver 80 comprises a first envelope detector 82 whose input is
15 connected receive one of the D_{OUT} signals. Specifically, envelope detector is
16 configured to detect the negative envelope or peaks of positive differential voltage
17 signal D^{+}_{OUT} and to create a first envelope voltage V_{1_ENV} indicating the negative
18 envelope of D^{+}_{OUT} .

19 The receiver 80 comprises feedback, associated with the described first
20 amplification stage, to adjust the gain of the first amplification stage to reduce the
21 difference between the first envelope voltage V_{1_ENV} and a supplied reference
22 voltage. As discussed above, the supplied reference voltage is preferably the
23 detected envelope voltage V_{C_ENV} of a related clock signal. As shown in Fig. 11,
24 clock signal $CLOCK$ is received by an envelope detector 84 to produce the
25 reference voltage V_{C_ENV} .

1 The feedback associated with the first amplification stage comprises a g_m
2 amplification stage or feedback component 86 whose output is connected to
3 control current source $I_{A_{BIAS}}$. The feedback adjusts the current through the first
4 amplification stage so that the negative envelope of D^{+}_{OUT} is approximately equal
5 to the negative envelope of clock signal CLOCK. This adjustment affects both of
6 the differential outputs D^{+}_{OUT} and D^{-}_{OUT} , although the negative envelope of the
7 D^{-}_{OUT} signal potentially exhibits the anomaly described with reference to Fig. 12.

8 Receiver 80 further comprises a second, singled-ended amplification stage
9 that affects the two differential outputs D^{+}_{OUT} and D^{-}_{OUT} unequally. Specifically,
10 this second amplification stage affects only the negative, D^{-}_{OUT} output of the
11 differential output pair.

12 The second amplification stage comprises a differential pair of transistors
13 M_{12} and M_{13} . The gate of M_{12} is controlled by D_{IN} and the gate of M_{13} is
14 controlled by V_{REF} . The sources of these two transistors are tied in common and
15 through a supplemental current source $I_{B_{BIAS}}$ to the lower supply voltage V_{ss} . The
16 drain of transistor M_{13} is connected to negative differential output D^{-}_{OUT} .
17 However, the drain of transistor M_{12} is connected directly to upper supply voltage
18 V_{dd} . Thus, this stage of amplification affects only negative differential output D^{-}_{OUT} .
19 The gain of this amplification stage is adjustable, and is controlled by current
20 source $I_{B_{BIAS}}$.

21 The circuit further comprises a second envelope detector 88 that is
22 responsive to the negative differential output signal D^{-}_{OUT} to produce a second
23 envelope voltage $V2_{ENV}$ reflecting the negative envelope or peaks of negative
24 differential output signal D^{-}_{OUT} . A g_m stage or feedback component 90 is
25 responsive to the $V1_{ENV}$ and $V2_{ENV}$ to adjust the gain of the second amplification

1 stage. Specifically, this feedback is configured to adjust the gain of the second
2 amplification stage to minimize the difference between the first and second
3 envelope voltages $V1_{ENV}$ and $V2_{ENV}$.

4 The two amplification stages, and the feedback associated with each
5 amplification stage, effectively adjust both the positive and negative components
6 of D_{OUT} to have amplitudes matching that of the clock signal $CLOCK$, and correct
7 for the asymmetrical differential output illustrated in Fig. 12.

8 Although Fig. 12 shows a receiver that receives only a single data signal,
9 the techniques shown in Fig. 13 can be used effectively in a receiver that receives
10 a plurality of signals. Fig. 13 shows such a receiver 100.

11 In Fig. 13, receiver 100 includes a plurality or group of signal receivers 102
12 such as described above with reference to Fig. 11. Each signal receiver
13 corresponds to and receives a single data input signal D_{IN} , and in response
14 produces a differential voltage output data signal D_{OUT} . Each receiver has a first
15 amplification stage that affects both the positive and negative components D^{+}_{OUT}
16 and D^{-}_{OUT} of the differential output. Each receiver also has a second
17 amplification stage that affects the first and second differential voltage data signals
18 unequally. Specifically, the second amplification stage of each receiver affects
19 only the negative, D^{-}_{OUT} differential output signal.

20 Receiver 100 includes a clock envelope detector 103 that is responsive to a
21 differential voltage clock signal to indicate a clock envelope voltage VC_{ENV} . In
22 this embodiment, the envelope detector is configured to detect the negative
23 envelope or peaks of the clock signal $CLOCK$.

24 Receiver 100 also includes first and second group envelope detectors 104
25 and 106. These detectors are like the group detectors previously discussed with

1 reference to Figs. 7 and 8, in that each detector is responsive to a collection of
2 signals to produce an envelope signal representing the most extreme envelope of
3 the collection or to produce an average of the envelopes of the signals. In this
4 embodiment, these envelope detectors are configured to detect the negative
5 envelopes or peaks of the respective signals.

6 More specifically, first group envelope detector 104 is responsive to the
7 collective positive differential voltage signals D^{+}_{OUT} to indicate a first group
8 envelope voltage $V1G_{ENV}$. Second envelope detector 106 is responsive to the
9 collective negative differential voltage signals D^{-}_{OUT} to indicate a second group
10 envelope voltage $V2G_{ENV}$.

11 Receiver 100 includes two feedback components 108 and 109. A first
12 feedback component or g_m stage 108 is configured to adjust the gain of the first
13 amplification stages of the individual signal receivers 102 to reduce or minimize
14 the difference between the first group envelope voltage $V1G_{ENV}$ and the clock
15 envelope voltage VC_{ENV} . A second feedback component or g_m stage 109 is
16 configured to adjust the gain of the second amplification stages of the individual
17 signal receivers 102 to reduce or minimize the difference between the first group
18 envelope voltage $V1G_{ENV}$ and the second group envelope voltage $V2G_{ENV}$.

19 The various exemplary embodiments described above illustrate the use of
20 real-time feedback to match both individual and group envelope voltages.
21 Specifically, the described envelope detection circuitry operates continuously to
22 indicate group envelope voltages, and the AGC feedback similarly operates in a
23 continuous mode in response to varying group envelope voltages. This is
24 appropriate in many situations, and especially in situations where point-to-point
25 data signaling is used. Such real-time feedback might not be appropriate in other

1 situations, however, especially those in which data might be received from a
2 plurality of different senders. In situations such as this, it might be more
3 appropriate to determine gains during calibration procedures performed while
4 receiving data from the different senders.

5 Fig. 14 shows pertinent components to implement an initialization
6 procedure to determine appropriate gains for use when receiving signals from
7 different senders. AGC feedback component 120 operates as described above with
8 reference to received individual or group envelope signals and produces an output
9 that adjusts the gain of an amplifier 122. A switching circuit 124 is configured
10 during the initialization procedure to supply the output of the AGC feedback
11 component 120 to the gain control input of amplifier 122. During initialization, an
12 appropriate data pattern is transmitted from the sending device and the AGC
13 feedback is allowed to reach a steady state. An analog-to-digital converter 124
14 samples the voltage output of feedback component 120 and converts it to a digital
15 value. This value is stored in storage elements or registers 126. This procedure is
16 repeated for different senders, and a gain value is stored for each sender.

17 During subsequent, normal operation, switching circuit 124 is configured to
18 supply a voltage produced by a digital-to-analog converter 128. Digital-to-analog
19 converter 128 receives its input from storage elements 126, which are controlled to
20 output a value that corresponds to the particular sending device that is currently
21 active.

22 Optionally, PVT (process, voltage, and temperature) correction can be
23 performed on the data before it is provided to digital-to-analog converter 128, as
24 shown by PVT correction component 130.
25

1 Fig. 15 shows an example of a g_m stage such as used in the circuits
2 described above, generally designated in Fig. 15 by reference numeral 200. The
3 g_m stage is preferably implemented digitally, so that PVT compensation and
4 calibration can be more easily accomplished.

5 The g_m stage 200 includes a comparator 202 that receives a reference signal
6 and a feedback signal. The comparator produces a positive or “true” output signal
7 when the voltage of the feedback signal is lower than that of the reference signal,
8 and a negative or “false” output signal when the voltage of the feedback signal is
9 higher than that of the reference signal.

10 A digital counter 204 receives the output of comparator 202 at its
11 increment/decrement input, labeled “+/-” in Fig. 15. Counter 204 is clocked at a
12 chosen frequency, and produces a digital output that varies as a function of the
13 output of comparator 202. If the output of comparator 202 is positive, the counter
14 increments its output at every clock cycle. If the output of comparator is negative,
15 the counter decrements its output at every clock cycle. In many embodiments, it
16 may be desirable to filter the signal from comparator 202 to reduce jitter. For
17 example, the circuit might be configured to require that the output of comparator
18 202 remain stable for a number of consecutive clock cycles before it is considered
19 valid, or before counter 204 will respond to it. “Majority” filtering might
20 alternatively be used, wherein a number of consecutive samples are collected and
21 the majority value of the samples is used as the filtered output.

22 The digital output of counter 204 is received by a digital-to-analog
23 converter (DAC) 206, where it is converted to an analog output signal.

24 This circuit produces an analog output voltage that varies in response to the
25 reference and feedback signals. At equilibrium, the output voltage will be such

1 that the reference and feedback signals are approximately equal, assuming that the
2 feedback signal is related in some positive manner to the output voltage.

3 The circuits and techniques describe above provide improvements in
4 automatic gain control. By collectively adjusting the gains of each data byte or
5 word, I/O line-to-line skew is minimized. Mismatches between the signal lines of
6 different bytes are minimized by adjusting different bytes or words to a common
7 reference. Furthermore, the techniques can be generalized to match the group
8 envelope of one type of data to the group envelope of some other type of data.

9 Although details of specific implementations and embodiments are
10 described above, such details are intended to satisfy statutory disclosure
11 obligations rather than to limit the scope of the following claims. Thus, the
12 invention as defined by the claims is not limited to the specific features described
13 above. Rather, the invention is claimed in any of its forms or modifications that
14 fall within the proper scope of the appended claims, appropriately interpreted in
15 accordance with the doctrine of equivalents.